IN THE CLAIMS

The following list of claims replaces all previous versions of the claims.

1. (Cancelled)

2. (Cancelled).

3. (Currently Amended) The method of claim ~~1~~ 24 wherein said communicating is selected from the group consisting of writing data to a location within said slave device and reading data from a location within said slave device.

4. (Cancelled)

5. (Cancelled).

6. (Cancelled).

7. (Cancelled).

8. (Cancelled).

9. (Currently Amended) The method of claim ~~8~~ 25 wherein said communicating comprises a write operation being performed from said master device to said slave device, said method further comprising the steps of:

transitioning to a receive state responsive to receipt of said command code;

receiving data transmitted from said master device; and,

writing said data to the slave device at a location therein identified by said 6-bit internal address.

10. (Cancelled).

11. (Cancelled).

12. (Cancelled).

13. (Cancelled).

14. (Cancelled).

15. (Previously presented) A method for a master device to communicate with a slave device connected to said master device via an inter-integrated circuit bus (I2C bus); said method comprising the steps of:

generating an array of addressing parameters comprising an address of said slave device followed by a command code comprising at least one indicator bit indicating the format of an internal address portion of the array, and at least a portion of said internal address followed by at least one array entry corresponding to said internal address;

wherein said at least one indicator bit is in either a first state or a second state;

when said at least one indicator bit is in said first state, utilizing some of the command code as part of said internal address, and utilizing an additional portion of said array as the remainder of said internal address; and

when said at least one indicator bit is in said second state, utilizing some of the command code as all of said internal address; and

transmitting said array over said I2C bus.

16. (Cancelled)

17. (Cancelled)

18. (Previously Presented) The method of claim 15 wherein said communication is selected from the group consisting of writing data to a location within said slave device and reading data from a location within said slave device and wherein, when said communication is a writing, said method further comprising the step of transmitting data over said I2C bus.

19. (Cancelled)

20. (Original) The method of claim 15 wherein;

said command code comprises 8 bits;

the at least one indicator bit comprises the 2 high order bits of said command code;

when said 2 high order bits are in said first state, the 6 low order bits of said command code comprise part of a 14-bit internal address, and an additional 8 bits of data in said array comprise the remainder of the 14-bit internal address; and

when said 2 high order bits are in said second state, the 6 low order bits of said command code comprise all of a 6-bit internal address.

21. (Original) The method of claim 20 wherein;

said 2 high order bits of said command code have a third state; and

when said 2 high order bits are in said third state, the 6 low order bits of said command code comprises an internal address associated with a particular register in said slave device that, when accessed, will cause the loading of predetermined data into said register via a hard-coded internal write operation.

22. (Cancelled).

23. (Cancelled).

24. (New) A method for communicating between a master device and a slave device connected via an inter-integrated circuit bus (I2C bus), said slave device comprising at least one internal device having an internal address, said method comprising the steps of:

sending a message from said master device to said slave device over said I2C bus;

said message comprising a command code to said addressed slave device, said command code comprising 8 bits, a 2-bit subset of said 8 bits functioning as an indicator of a type of supplemental address that is being provided, wherein a particular state of said 2-bit indicator indicates that the supplemental address contains 6 bits of a 14-bit internal address that is being provided;

said slave device determining whether the 2-bit indicator is in said particular state, and, if said 2-bit indicator is in said particular state, said slave device utilizing the 6 low order bits of the command code as part of the 14-bit internal address and an additional 8 bits of data as the remainder of the 14-bit internal address.

25. (New) A method for communicating between a master device and a slave device connected via an inter-integrated circuit bus (I2C bus), said slave device comprising at least one internal device having an internal address, said method comprising the steps of:

sending a message from said master device to said slave device over said I2C bus;

said message comprising a command code to said addressed slave device, said command code comprising 8 bits, a 2-bit subset of said 8 bits functioning as an indicator of a type of supplemental address that is being provided, wherein a particular state of said 2-bit indicator indicates that the supplemental address contains 6 bits of a 6-bit internal address that is being provided:

said slave device determining whether the 2-bit indicator is in said particular state, and, if said 2-bit indicator is in said particular state, said slave device utilizing the 6 low order bits of the command code as the 6-bit internal address.

26. (New) The method of claim 25 wherein said communicating is selected from the group consisting of writing data to a location within said slave device and reading data from a location within said slave device.

27. (New) A method for communicating between a master device and a slave device connected via an inter-integrated circuit bus (I2C bus), said slave device comprising at least one internal device having an internal address, said method comprising the steps of:

sending a message from said master device to said slave device over said I2C bus;

said message comprising a command code to said addressed slave device, said command code comprising 8 bits, a 2-bit subset of said 8 bits functioning as an indicator of a type of supplemental address that is being provided, wherein a particular state of said 2-bit indicator indicates that a direct write operation of data is being performed to a particular register in the slave device;

said slave device, responsive to said 2-bit indicator being in said particular state, parsing the 6 low order bits of the command code to obtain said internal address which, when accessed, will cause the loading of predetermined data into said register via a hard-coded internal write operation.

28. (New) The method of claim 27 wherein said communicating is selected from the group consisting of writing data to a location within said slave device and reading data from a location within said slave device.

29. (New) A method for communicating between a master device and a slave device connected via an inter-integrated circuit bus (I2C bus), said slave device comprising at least one internal device having an internal address, said method comprising the steps of:

sending a message from said master device to said slave device over said I2C bus;

said message comprising a command code to said addressed slave device, said command code comprising 8 bits, a 2-bit subset of said 8 bits functioning as an indicator of a type of supplemental address that is being provided, wherein said 2-bit indicator being in a first state indicates that one of a 6-bit supplemental address that is used as part of a communicated 14-bit internal address is being provided and said 2-bit indicator being in a second state indicates that a 6-bit supplemental address that is used as a 6-bit internal address is being provided;

said slave device interpreting said supplemental address contained in said command code in accordance with said state of said two bit indicator; and

said slave device determining an internal address for said slave device using said supplemental address.

30. (New) The method of claim 29 wherein said communicating is selected from the group consisting of writing data to a location within said slave device and reading data from a location within said slave device.

31. (New) A method for communicating between a master device and a slave device connected via an inter-integrated circuit bus (I2C bus), said slave device comprising at least one internal device having an internal address, said method comprising the steps of:

sending a message from said master device to said slave device over said I2C bus;

said message comprising a command code to said addressed slave device, said command code comprising 8 bits, a 2-bit subset of said 8 bits functioning as an indicator of a type of supplemental address that is being provided, wherein said 2-bit indicator being in a first state indicates that a 6-bit supplemental address that is used as part of a communicated 14-bit internal address is being provided and said 2-bit indicator being in a second state indicates that a 6-bit supplemental address that is used as a 6-bit internal address for a direct command access operation is being provided;

said slave device interpreting said supplemental address contained in said command code in accordance with said state of said two bit indicator; and

said slave device determining an internal address for said slave device using said supplemental address.

32. (New) The method of claim 31 wherein said communicating is selected from the group consisting of writing data to a location within said slave device and reading data from a location within said slave device.

33. (New) A method for communicating between a master device and a slave device connected via an inter-integrated circuit bus (I2C bus), said slave device comprising at least one internal device having an internal address, said method comprising the steps of:

sending a message from said master device to said slave device over said I2C bus;

said message comprising a command code to said addressed slave device, said command code comprising 8 bits, a 2-bit subset of said 8 bits functioning as an indicator of a type of supplemental address that is being provided, wherein said 2-bit indicator being in a first state indicates that a 6-bit supplemental address that is used as a 6-bit internal address is being provided and said 2-bit indicator being in a second state indicates that a 6-bit supplemental address that is used as a 6-bit internal address for a direct command access operation is being provided;

said slave device interpreting said supplemental address contained in said command code in accordance with said state of said two bit indicator; and

said slave device determining an internal address for said slave device using said supplemental address.

34. (New) The method of claim 33 wherein said communicating is selected from the group consisting of writing data to a location within said slave device and reading data from a location within said slave device.

35. (New) A method for communicating between a master device and a slave device connected via an inter-integrated circuit bus (I2C bus), said slave device comprising at least one internal device having an internal address, said method comprising the steps of:

sending a message from said master device to said slave device over said I2C bus;

said message comprising a command code to said addressed slave device, said command code comprising 8 bits, a 2-bit subset of said 8 bits functioning as an indicator of a type of supplemental address that is being provided, wherein said 2-bit indicator being in a first state indicates that a 6-bit supplemental address that is used as part of a communicated 14-bit internal address is being provided, said 2-bit indicator being in a second state indicates that a 6-bit supplemental address that is used as a 6-bit internal address is being provided, and said 2-bit indicator being in a third state indicates that a 6-bit supplemental address that is used as a 6-bit internal address for a direct command access operation is being provided;

said slave device interpreting said supplemental address contained in said command code in accordance with said state of said two bit indicator; and

said slave device determining an internal address for said slave device using said supplemental address.

36. (New) The method of claim 35 wherein said communicating is selected from the group consisting of writing data to a location within said slave device and reading data from a location within said slave device.